

Fig. 1

Fig. 2

<u>Fig. 3</u>

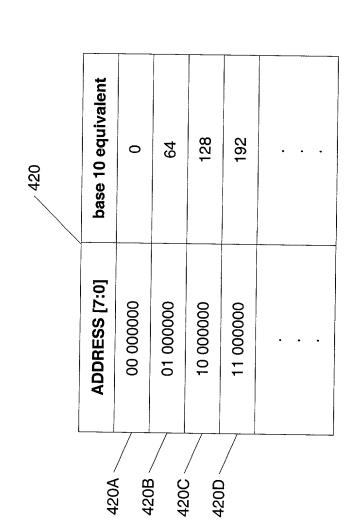
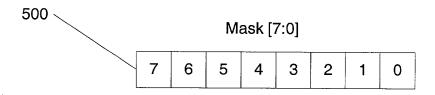


Fig. 4



	502	
504A	Mask Bit	Block Bytes
504B	0	0-7
504C	1	8-15
504D	2	16-23
504E	3	24-31
504F	4	32-39
504G	5	40-47
504H	6	48-55
	7	56-63

Fig. 5

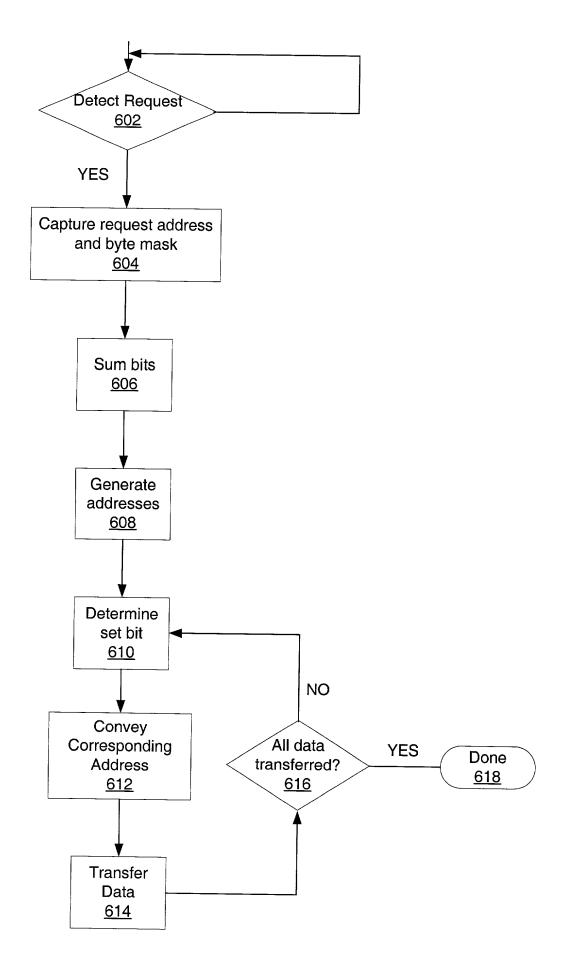


Fig. 6

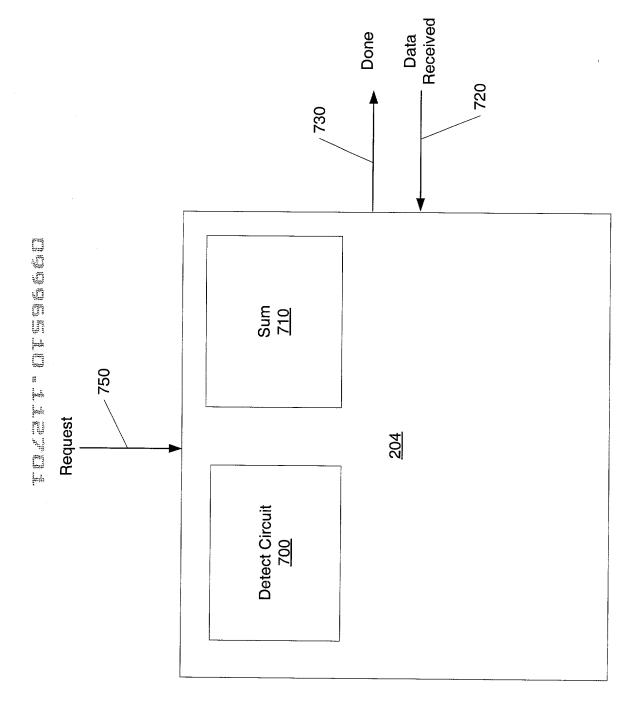


Fig. 7

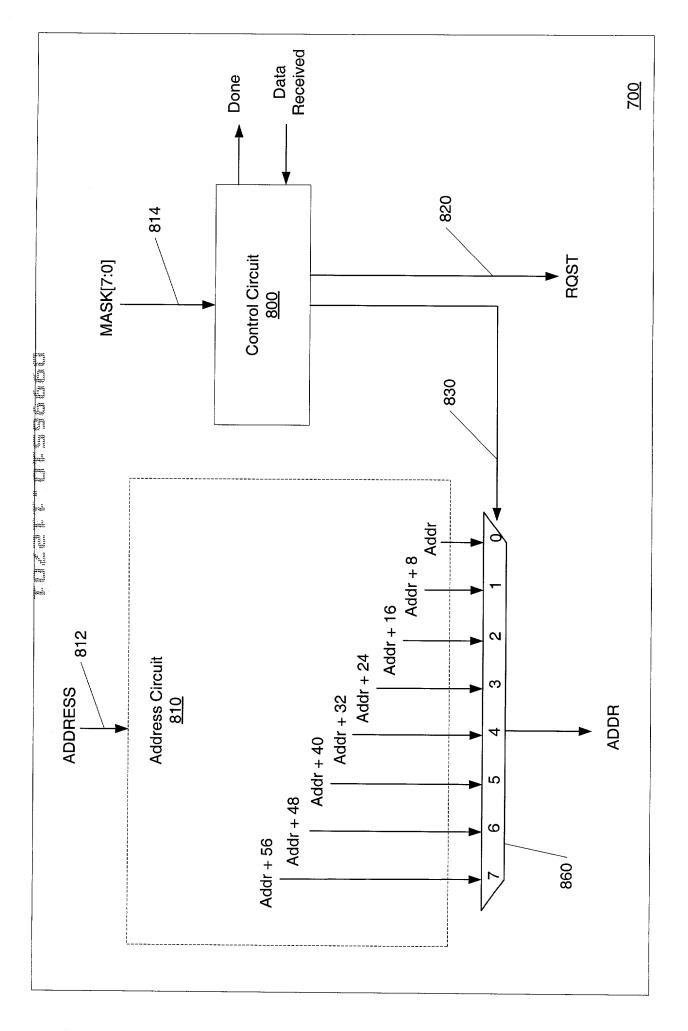
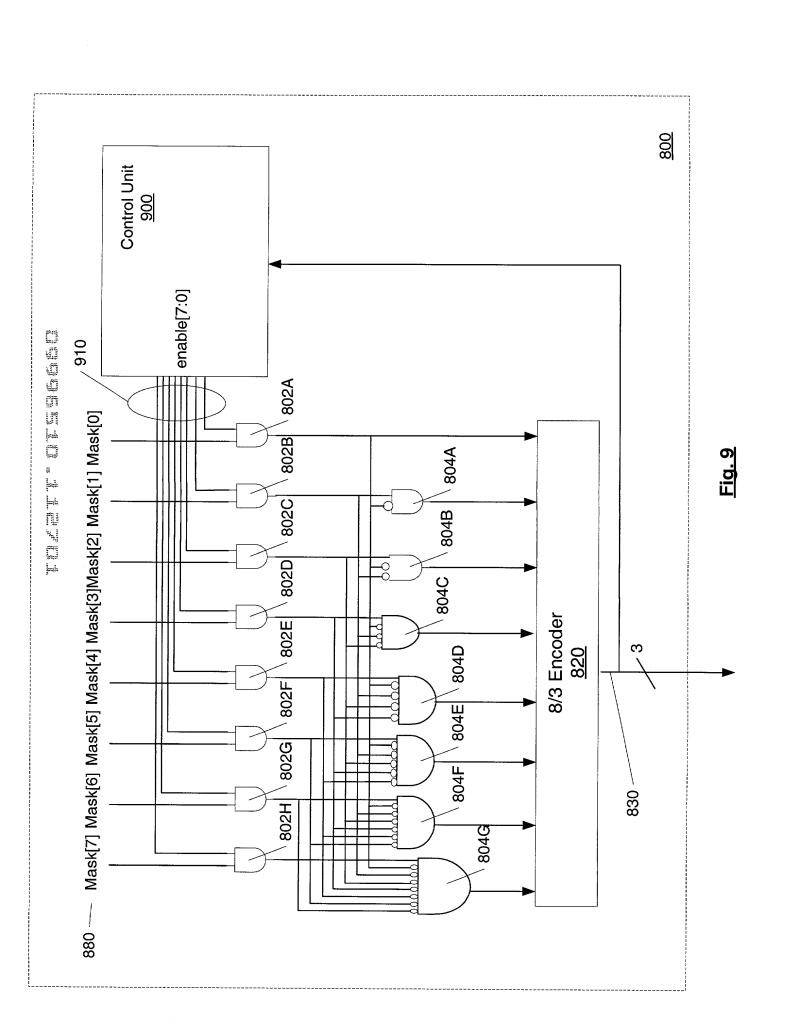


Fig. 8



Iteration 1002	Enable[7:0] <u>1004</u>	Mask[7:0] <u>1006</u>	gates 802H-802A 1008	gates 804G-804A 1010	signal[2:0] 830 <u>1012</u>
0	11111111	01101000	01101000	00001000	011
•	11110000	01101000	01100000	00100000	101
Ø	11000000	01101000	01000000	01000000	110

Fig. 10